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METHOD TO FORM COPPER SEED LAYER FOR COPPER INTERCONNECT

FIELD OF THE INVENTION

The invention relates to the general field of integrated circuits with particular reference to copper based damascene connectors.

BACKGROUND OF THE INVENTION

Integrated circuits are widely used in electronic devices of many types. Conventional aluminum and aluminum alloys have been widely used as interconnection materials for integrated circuits. However, the downscaling of metal interconnect lines and the increase in electrical current density result in greater RC time delay along with enhanced electromigration and stress induced V_{bid} failures. To solve these functionality and reliability problems, an intense research effect has been focused on copper metalization due to its low bulk resistivity (1.68 μohm cm for Cu, compared to 2.7 μohm cm for Al), excellent electro-migration resistance, and high resistance to stress. However, copper metalization processes require a copper seed layer which is thin and has conformal step-coverage for eletroplating (ECP) or physical vapor deposition (PVD) trench-fill. The quality of the copper seed layer strongly affect the properties of the film that fills the trench, including crystalline quality, film adhesion strength, stress, and reliability within integrated circuits.

PVD Cu is known to be one of the best techniques for depositing a Cu seed layer due to its good physical step-coverage, good adhesion strength, particularly to diffusion barrier metal layer such as TiN , Ta and TaN. However, PVD Cu processes have been found to be less suitable when it becomes necessary to obtain uniform coverage of high aspect ratio trench and via side walls of the type seen in dual damascene structures. In this respect, Chemical Vapor Deposition (CVD) techniques have an advantage since they are able to achieve a high level of step-coverage (>80%).

CVD would therefore appear to be the technique of choice for Cu seed layer formation, particularly for next generation dual damascene technology. However, the Cu adhesion strength to the underneath layer (typically a diffusion barrier layer) is bad, it not being able even to pass the standard Scotch tape test. The grain structure of CVD Cu seed layers is another important factor. The surface roughness of CVD Cu seed layers may cause non uniform growth of subsequently deposited ECP Cu films, resulting in voids and incomplete gap filling. The texture of a CVD Cu seed also influences Cu interconnection failure induced by electromigration (EM) when applying higher current densities in ultra large scale integration circuits. It is well known that a <111> crystalline texture, including barrier layer and Cu film, brings improved Cu interconnections and increases EM endurance. However, CVD Cu seed layers tend to have a preferred <200> orientation rather than a <111> when deposited on some barrier materials.

Currently, PVD Cu remains the technique of choice for preparing Cu seed layers but CVD Cu processes are being considered for the next generation, because of its superior step coverage. The present invention discloses how CVD Cu may be used while at the same time, having good adhesion and a <111> preferred orientation.

A routine search of the prior art was performed with the following references of interest being found:

In US 2002-011,965,711 Gandikota et al. show a Cu process with a metal plasma CVD nucleation layer. In US 2002-0,068,449 A1 Hashim et al. disclose a Cu seed layer process with a metal plasma CVD nucleation layer while in US 6, 391,776 B2 Hashim et al. disclose a Cu seed layer process. Brown shows a Cu dual damascene process with a barrier layer in US 6,306,732 B1.

SUMMARY OF THE INVENTION

It has been an object of at least one embodiment of the present invention to provide a method of forming a copper seed layer, having good step coverage, for a copper metalization interconnection in semiconductor integrated circuits.

Another object of at least one embodiment of the present invention has been to allow a seed layer for copper metalization to be formed using standard CMOS process steps with dual damascene technology.

Still another object of at least one embodiment of the present invention has been that said seed layer have good adhesion to the barrier layer used with said damascene technology.

A further object of at least one embodiment of the present invention has been that said seed layer have good lattice continuity relative to said barrier layer, thereby increasing the electromigration resistance of the structure.

These objects have been achieved by preceding the deposition of the CVD copper layer with a very thin copper layer that was deposited using an ionized metal plasma at -40 C followed by treatment in a nitrogen bearing plasma. The result is a seed layer having excellent step coverage as well as very good adhesion to the underlying barrier layer. Instead of the <200> crystalline orientation normally obtained with CVD seed layers of the prior art (when deposited on some metals), a <111> orientation is obtained, making for improved lattice continuity with the barrier layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the initial layered structure that is to be processed.

FIG. 2 is FIG. 1 after a via hole has been etched.

FIG. 3 is FIG. 2 after a trench has been etched and cleaned using plasma and chemical means.

Fig. 4 illustrates the deposition of a barrier layer followed by application of a metal plasma treatment.

Fig. 5 illustrates the application of a nitrogen plasma treatment to FIG. 4 followed by deposition of a CVD Cu layer.

FIG. 6A plots room temperature residual stress as a function of PVD Cu plasma treatment time for Cu films deposited by CVD.

FIG. 6B plots non-uniformity of sheet resistance as a function of the duration of said metal plasma treatment.

FIG. 7 plots adhesion of the seed layer as a function of the duration of said metal plasma treatment.

FIG. 8 compares several X-ray diffraction spectra as a function of the duration of said metal plasma treatment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

We will illustrate the process of the present invention through a description of its application to filling damascene trenches and vias, but it will be clear to all skilled in the art that the invention is more general than this and may be applied to copper coating of other, non-planar surfaces. Referring now to FIG. 1, the process begins with the provision of partially completed integrated circuit 10 onto whose top surface are deposited, in succession, etch stop layer 11, dielectric layer 15, etch stop layer 12, dielectric layer 16, and cap layer 13. Suitable materials for layers 15 and 16 include silicon oxide, black diamond (methyl-doped porous silica), CORAL (carbon doped silicon oxide), PORA (carbon doped silicon oxide), and SiLK (low k organic polymer), while for the etch stop and cap layers, suitable materials include silicon nitride and silicon carbide.

The next step, as shown in FIG. 2, is to etch via 21 that extends as far as etch stop layer 11. Typically, via 21 has a depth of between about 0.5 and 1.3 microns and a diameter of between about 0.1 and 0.3 microns. Then trench 31 is etched. It extends

down as far as etch stop layer 12 and has a depth of between about 0.25 and 0.5 microns and a width of between about 0.1 and 0.3 microns. Then, etch stop layers 11 and 12 and cap layer 13 are etched, following which plasma and chemical treatments are used to strip polymer residues. Following this, all exposed surfaces are coated with barrier layer 32 which is a refractory metal such as Cr, Nb, Ti, Mo, W, or Ta, or one of their nitrides. The appearance of the structure at this stage is shown in FIG. 3.

Now follows a key feature of the invention, namely the use of a metal plasma technique (such as RF, DC, or magnetron sputtering and symbolized by arrows 42 in FIG. 4) to deposit very thin layer of copper 41 on barrier layer 32 while maintaining the latter (in practice the entire structure) at a temperature less than about -40 C. This metal plasma technique is applied for between about 2 and 10 seconds which results in a copper film whose thickness is between about 10 and 50 Angstroms. Layer 41, when deposited under these conditions, is found to have a preferred <111> crystalline orientation.

Copper layer 41 is then exposed to a nitrogen bearing plasma, as symbolized in FIG. 5 by arrows 52. Examples of suitable gases used to generate this nitrogen bearing plasma include (but are not limited to) nitrogen, ammonia, or forming gas (nitrogen + about 10% hydrogen). To generate the nitrogen bearing plasma, one of these gases is taken to a pressure between about 1×10^{-2} and 6×10^{-2} torr and a plasma is electrolessly excited therein at a power level of between about 100 and 300 watts. The plasma is typically applied for between about 5 and 30 seconds.

Following the plasma treatment, a second (and thicker) layer of copper 51 is laid down by means of chemical vapor deposition. Our preferred process for this includes use of Cupraselect (trimethyl-vinyl-silyl hexafluoro-acetylacetonate copper} along with products such as Hfac (hexafluoroacetyl acetonate dihydride) and TMVS (trimethyl vinyl silane), only under optimized conditions, and layer 51 is deposited to a thickness of between about 200 and 800 Angstroms. Under these deposition conditions, layer 51 ends up achieving a step coverage of at least 90 %. Additionally, the non-uniformity of layer 51 was improved from about 11% down to about 4% (based on sheet resistance measurements)

This completes formation of the seed layer onto which additional copper may then be deposited through electroplating until via hole 21 and trench 31 are completely filled with copper, thus forming the dual damascene structure.

RESULTS

1)Stress and sheet resistance measurements:

FIG. 6A shows the residual stress (at room temperature), as a function of the preceding PVD Cu plasma treatment time, for Cu films deposited by CVD. The film thickness was fixed at 150 nm to eliminate thickness as a variable. The residual stress of CVD Cu films is tensile. Without the PVD Cu plasma treatment, the structure was essentially amorphous, at the CVD Cu and barrier layer interface, having large pores and voids, indicating a lower tensile stress level. As the PVD Cu plasma treatment time

increased, the tensile stress also increased (became more negative), probably due to smaller pores and voids and a better inter-connected atomic network. When the PVD Cu plasma treatment was long enough (about 2 seconds), the amorphous-like layer disappeared and was replaced by epitaxially grown copper with larger grains. It appears that the PVD Cu plasma treatment provides nucleation centers for the subsequent CVD Cu deposition. As shown in FIG. 6B, The non-uniformity of CVD Cu films (based on sheet resistance measurements) was improved from about 11% down to about 4%

2) Adhesion measurements:

The adhesion strength of the copper layer 41 to the barrier layer layer 32 (see FIG. 4) was good enough to pass the standard Scotch tape test. In contrast, a CVD Cu layer film deposited directly on the diffusion barrier metal layer could not pass this relatively mild test. Auger analysis results showed that the failure occurred at the CVD copper- barrier layer interface. However, all CVD Cu films prepared as described above (i. e. with a preceding PVD Cu plasma treatment) could pass the standard Scotch tape test.

This is illustrated in FIG. 7 where the adhesion of CVD films (normalized relative to Cu CVD films deposited according to the prior art) has been plotted as a function of the duration of the metal plasma treatment. As can be seen, a metal plasma treatment of only about two seconds is sufficient to more than double the relative adhesion. Expressed in absolute units, the adhesion of the CVD films (deposited in accordance with the process of the present invention) exceeded 650 N in a stud pull test.

3) X-ray diffraction (XRD):

Figure 8 compares the XRD patterns for CVD Cu films after various treatment times to the PVD Cu plasma. FIG. 81 is for no pre-treatment, FIG. 82 for a one second metal plasma treatment and FIG. 83 is for a two second treatment. No noticeable changes can be observed for the TaN peak (from the barrier layer) with or without PVD Cu plasma treatment. However, the copper <111> peak is seen to have increased significantly with plasma pre-treatment while the copper <200> peak has become weaker. This confirms that the PVD Cu under-layer is effective to enhance the CVD Cu <111> texture, implying an enhancement of lattice continuity between the CVD Cu layer and the barrier layer. This serves to increase the electro-migration resistance of the structure. A Siemens XRD system used to generate the data.

What is claimed is: